Am27S23/Am27S23A

2,048-Bit (256x8) Bipolar PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

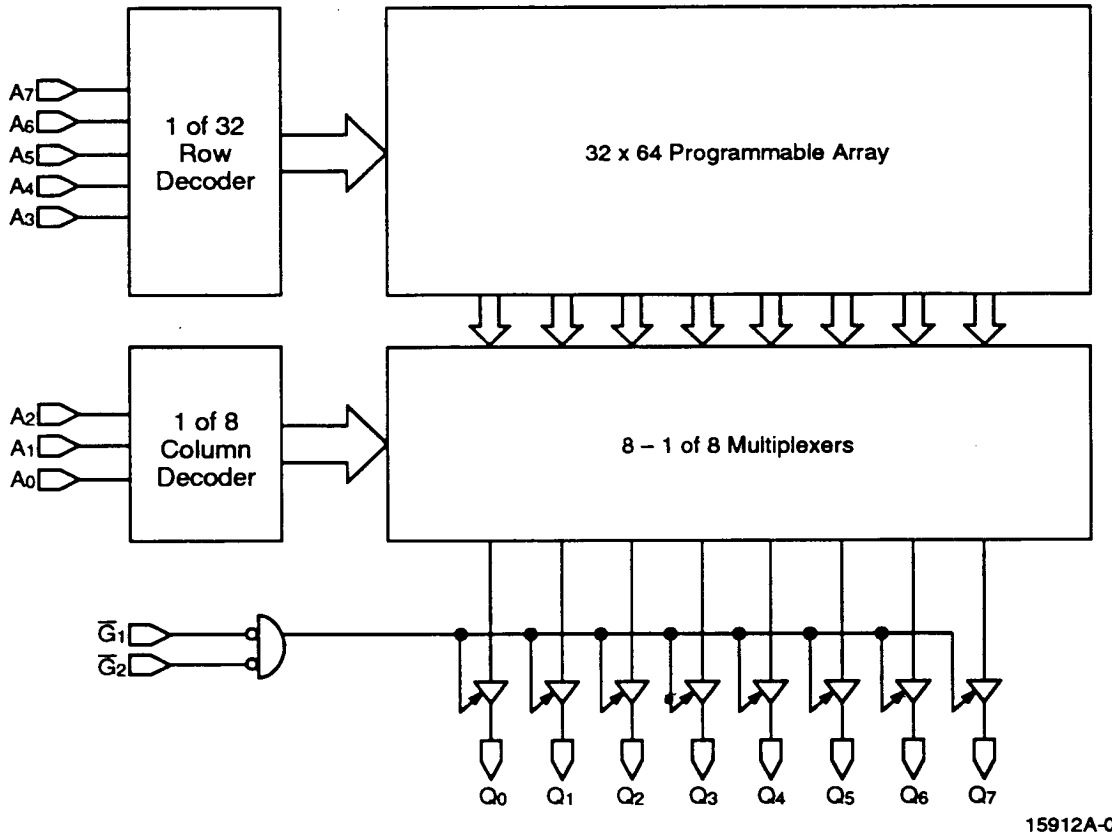
- **High Speed**
- **Highly reliable, ultra-fast programming Platinum-Silicide fuses**
- **High programming yield**
- **Low-current PNP inputs**
- **High-current open-collector and three-state outputs**
- **Fast chip select**

GENERAL DESCRIPTION

The Am27S23 (256-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs, compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word depth expansion is facilitated by active LOW ($\overline{G}_1$, $\overline{G}_2$) output enables.

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Three-State Part Number	Am27S23A		Am27S23	
Address Access Time	30 ns	40 ns	45 ns	50 ns
Operating Range	C	M	C	M

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Issue Date: August 1991

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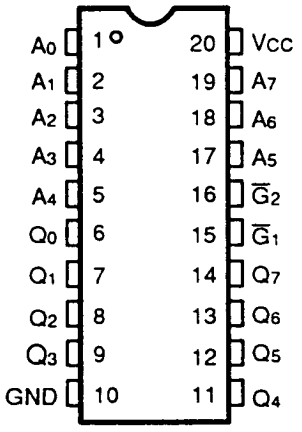
CONNECTION DIAGRAMS
Top View

DIPs*



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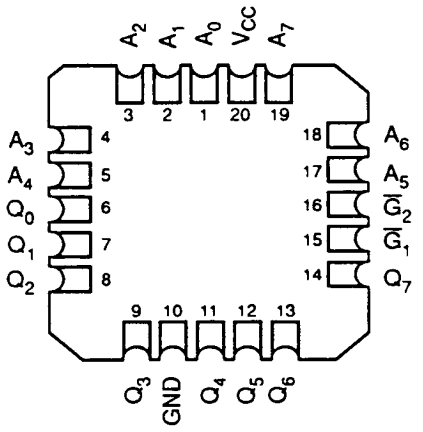
LCC**



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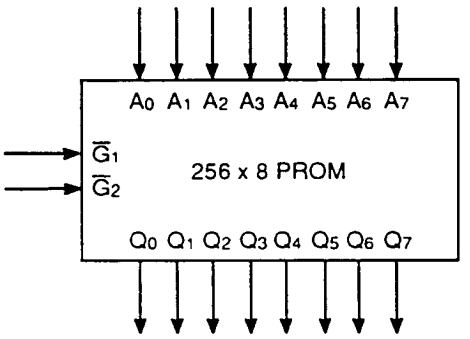
Note: Pin 1 is marked for orientation.

*Also available in a 20-pin Flatpack. Pinout identical to DIPs.

**Also available in a 20-pin PLCC. Pinout identical to LCC

LOGIC SYMBOL



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ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing

AM27S23 A P C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

TEMPERATURE RANGE
C = Commercial (0 to +75°C)

PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)
L = 20-Pin Ceramic Leadless Chip Carrier (CL 020)
J = 20-Pin Plastic Leaded Chip Carrier (PL 020)

SPEED OPTION
A = 30 ns
Blank = 45 ns

DEVICE NUMBER/DESCRIPTION
256 x 8 Bipolar PROMS
Am27S23 = Three State

Valid Combinations	
AM27S23	PC, PCB, DC, DCB, LC, LCB, JC, JCB
AM27S23A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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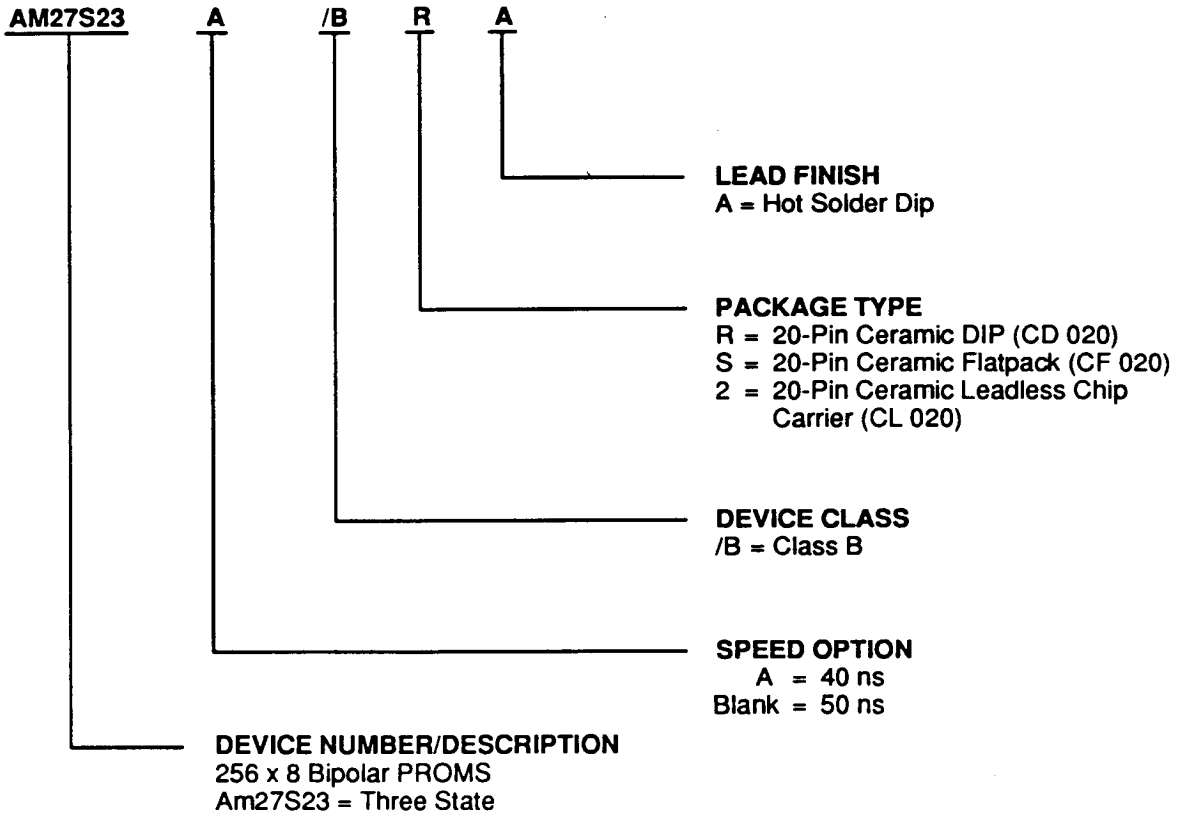
ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (if applicable)
Device Class
Package Type
Lead Finish



Valid Combinations	
AM27S23	/BRA, /BSA, /B2A
AM27S23A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A Tests consist of Subgroups:
1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

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PIN DESCRIPTION

$A_0 - A_7$
Address (Inputs)

The 9-bit field presented at the address inputs selects one of 256 memory locations to be read from.

$Q_0 - Q_7$
Data Output Port

The outputs whose state represents the data read from the selected memory locations.

$\overline{G}_1$, $\overline{G}_2$
Output Enables (Input)

Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$
Disable = G

V_{CC}
Device Power Supply Pin

The most positive of the logic power supply pins.

GND
Device Power Supply Pin

The most negative of the logic power supply pins.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming)	–0.5 V to V_{CC} Max.
DC Voltage Applied to Outputs During Programming	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec)	250 mA
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +75°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V

Military (M) Devices*

Case Temperature (T_C)	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and –55°C

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OH} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.50	V
V_{IH}	Input HIGH Level	Guaranteed input Logical HIGH voltage for all outputs (Note 2)	2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V			–0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			25	µA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)	–20		–90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.			160	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max, $V\overline{G}_1$ = 2.4 V, (Note 1), V_O = V_{CC}			40	µA
		V_{CC} = Max, $V\overline{G}_1$ = 2.4 V, (Note 1), V_{OUT} = 0.4 V			–40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4) V_{CC} = 5 V; T_A = 25°C		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4) V_{CC} = 5 V; T_A = 25°C		8		pF

Notes:

1. This applies to three-state devices only.
2. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

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SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		45		50	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		25		30		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		25		30		25		30	ns

See also Switching Test Circuits.

*Subgroups 7 and 8 apply to functional tests.

Notes:

1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure A.
2. TGVQZ is measured at steady state HIGH output voltage –0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in Figure B.

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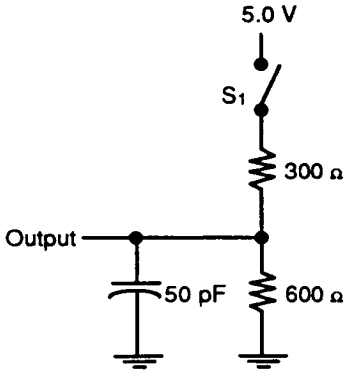
SWITCHING TEST CIRCUITS



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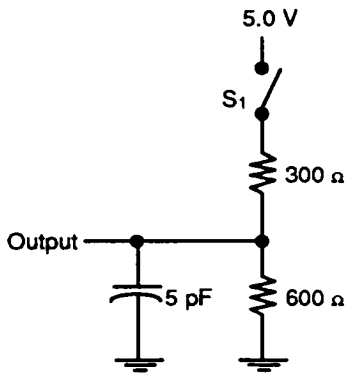
A. Output Load for all A – C Tests Except TGVQZ



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B. Output Load for TGVQZ

Notes:

1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data High to Hi-Z and Hi-Z to Output Data High tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

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KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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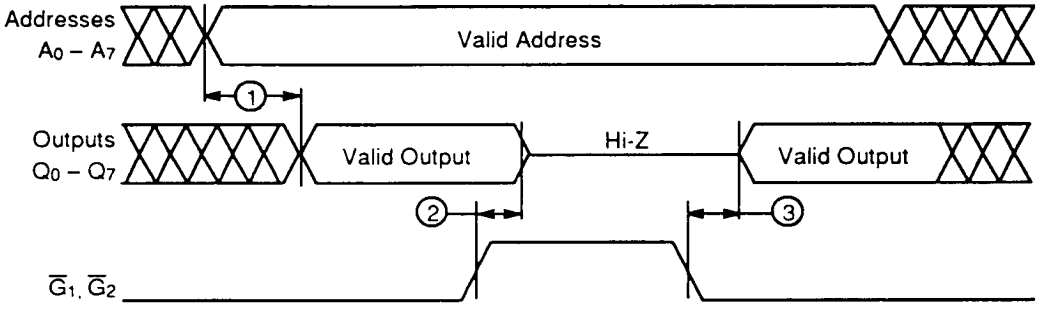

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